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What is claimed is:

1. An apparatus, comprising:
   a request queue coupled to a memory unit via a memory-sensing device;
   a response queue coupled to the memory-sensing device; and
   an arbiter coupled to said response queue.

2. The apparatus of claim 1, wherein the memory-sensing device comprises redundant circuitry capable of sensing memory in the memory unit substantially simultaneously.

3. The apparatus of claim 1, wherein said request queue comprises memory to store more than one request.

4. The apparatus of claim 3, wherein the memory to store more than one request comprises memory to service more than one request substantially simultaneously.

5. The apparatus of claim 1, wherein said response queue comprises memory to store data for a response.

6. The apparatus of claim 1, wherein said arbiter comprises a response arbiter to determine a response to more than one request.

7. The apparatus of claim 6, wherein the response arbiter comprises a priority determiner to determine a priority of a response to a request.

8. The apparatus of claim 1, wherein said arbiter comprises a request arbiter coupled to said request queue.

9. A method, comprising:

receiving more than one request for sensing data in a memory unit;

sensing data in the memory unit;

returning critical data in response to said receiving more than one request; and

returning non-critical data.

10. The method of claim 9 wherein said receiving more than one request for sensing data in a memory unit comprises receiving a second transaction before completing a response to a first transaction.

11. The method of claim 9 wherein said receiving more than one request for sensing data in a memory unit comprises receiving a request to read critical data.

12. The method of claim 9 wherein said sensing data in the memory unit comprises determining an order to sense data based on available redundant circuitry.

13. The method of claim 9 wherein said returning critical data comprises interrupting a response to a first request comprising non-critical data to return critical data in response to a second request.

14. The method of claim 9 wherein said returning non-critical data comprises returning non-critical data in accordance with a pre-defined protocol.

15. The method of claim 14 wherein returning non-critical data in accordance with a pre-defined protocol comprises responding to each request of the more than one request with time-sliced burst data.

16. The method of claim 14 wherein returning non-critical data in accordance with a pre-defined protocol comprises returning non-critical data in an order based upon a priority attached to the more than one request.

17. A system, comprising:
    a virtual-port memory device;
    a memory controller coupled to said virtual-port memory device; and
    a host coupled to said memory controller.

18. The system of claim 17, wherein said virtual-port memory device comprises:
    a request queue coupled to a memory unit via a memory sensing device;
    a response queue coupled to the memory sensing device; and
    an arbiter coupled to said response queue.

19. The system of claim 18, wherein the arbiter comprises a response arbiter to determine a response to more than one request.

20. The system of claim 17, wherein said memory controller comprises:
    a response interpreter coupled to said virtual-port memory device;
    a host response queue coupled to the response interpreter; and
    a host request queue coupled to said host.

21. A system, comprising:
a virtual-port memory device coupled to a microprocessor; and
an input-output device coupled to the microprocessor.

22. The system of claim 21, wherein said virtual-port memory device comprises:
a request queue coupled to a memory unit via a memory sensing device;
a response queue coupled to the memory sensing device; and
an arbiter coupled to said response queue.

23. The system of claim 21, wherein said input-output device comprises an antenna device.

24. The system of claim 21, wherein said input-output device comprises an audio input device and an audio output device.

25. A machine-readable medium containing instructions, which when executed by a machine, cause said machine to perform operations, comprising:

receiving more than one request for sensing data in a memory unit;

sensing data in the memory unit;

returning critical data in response to said receiving more than one request; and

returning non-critical data.

26. The machine-readable medium of claim 25 wherein said receiving more than one request for sensing data in a memory unit comprises receiving a second transaction before completing a response to a first transaction.

27. The machine-readable medium of claim 25 wherein said receiving more than one request for sensing data in a memory unit comprises receiving a request to read critical data.

28. The machine-readable medium of claim 25 wherein said sensing data in the memory unit comprises determining an order to sense data based on available redundant circuitry.

29. The machine-readable medium of claim 25 wherein said returning critical data comprises interrupting a response to a first request comprising non-critical data to return critical data in response to a second request.

30. The method of claim 25 wherein said returning non-critical comprises returning non-critical data in accordance with a pre-defined protocol.

31. An apparatus, comprising:
    a memory unit;
    a memory-sensing device coupled with said memory unit;
    a request queue coupled with said memory sensing device to receive more than one request to sense data in said memory unit; and
    an arbiter coupled with said memory sensing device to determine the sequence to return the data in response to the more than one request.

32. The apparatus of claim 31, further comprising a response queue coupled with said memory sensing device to store the data.

33. The apparatus of claim 31, wherein said memory unit comprises a first partition and a second partition; and said memory-sensing device comprises redundant circuitry coupled with said memory unit to sense data in the first partition and the second partition substantially simultaneously.

34. The apparatus of claim 31, wherein said request queue comprises memory to store the more than one request.

35. The apparatus of claim 31, wherein said arbiter comprises a response arbiter coupled with said memory sensing device to determine a response to the more than one request.

36. The apparatus of claim 35, wherein the response arbiter comprises a priority determiner to determine a priority of the response to the more than one request.

37. The apparatus of claim 31, wherein said arbiter comprises a request arbiter coupled with said request queue to determine a priority to sense data in response to the more than one request.

38. A system, comprising:
a memory unit;
a memory-sensing device coupled with said memory unit;
a request queue coupled with said memory sensing device to receive more than one request to sense data in said memory unit; and
an arbiter coupled with said memory sensing device to determine the sequence to return the data in response to the more than one request; and
a processor coupled with said request queue to initiate a first request of the more than one request.

39. The system of claim 38, further comprising a memory controller coupled between said request queue and said processor.

40. The system of claim 38, further comprising an input-output device.